TSD9926B

20V Dual N-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The XP9926B is the N-Channel logic enhancement mode power field effect transistor, is produced using high cell density advanced trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits.

■ *FEATURE*

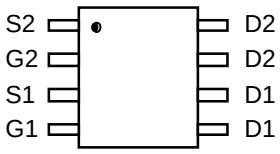
- ***20V/8.0A, $R_{DS(ON)}$=15mΩ (typ.)@VGS= 10V***
- ***20V/7.0A, $R_{DS(ON)}$=17mΩ (typ.)@VGS= 4.5V***
- ***20V/6.0A, $R_{DS(ON)}$=22mΩ (typ.)@VGS= 2.5V***
- ***20V/2.0A, $R_{DS(ON)}$=30mΩ (typ.)@VGS= 1.8V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design

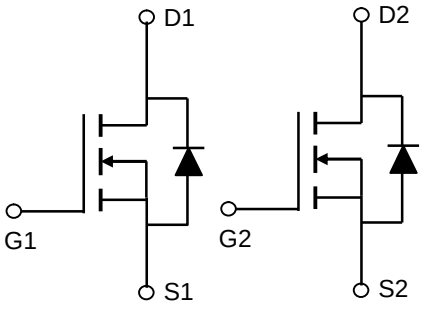
■ *APPLICATIONS*

- Power Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

■ *PIN CONFIGURATION*

Top View





■ *PART NUMBER INFORMATION*

XP 9926BA-BB C	A= Package Code S: SOP BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ *ORDERING INFROMATION*

Part Number	Package Code	Package	Shipping
XP9926B S-TRG	S	SOP8	3000EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

■ *ABSOLUTE MAXIMUM RATINGS* (T_A = 25℃ *Unless otherwise noted*)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [A]	T_A=25℃	I_D	8.0	A
	T_A=70℃		6.1	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	62.5	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		73	110	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	31	40	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

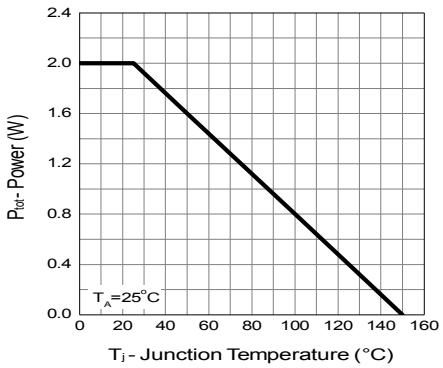
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250uA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= 250uA	0.4	0.75	1.1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 20V, V_{GS}=0			1	uA
		V_{DS}= 20V, V_{GS}=0 T_J=55℃			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}= 10V, I_D= 8.0A		15	23	mΩ
		V_{GS}= 4.5V, I_D= 7.0A		17	26	
		V_{GS}= 2.5V, I_D= 6.0A		22	34	mΩ
		V_{GS}= 1.8V, I_D= 2.0A		30	52	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= 1.0A, V_{GS}=0V		0.8	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}= 15V V_{GS}= 10V I_D= 7.6A		15.6		nC
Q_{gs}	Gate-Source Charge			1.3		
Q_{gd}	Gate-Drain Charge			2.5		
C_{iss}	Input Capacitance	V_{DS}= 15V V_{GS}=0V f=1MHz		520		pF
C_{oss}	Output Capacitance			105		
C_{rss}	Reverse Transfer Capacitance			60		
$T_{d(on)}$	Turn-On Time	V_{DS}= 15V I_D= 1A V_{GEN}= 10V R_G=3Ω		4		nS
T_r				6		
$T_{d(off)}$	Turn-Off Time			25		
T_f				4		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

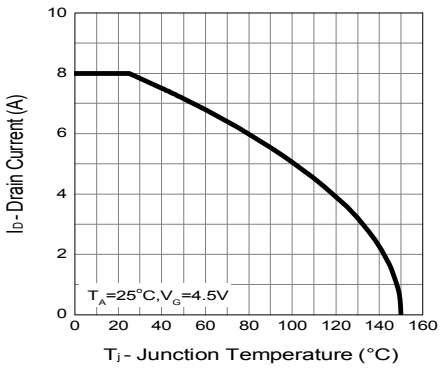
2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

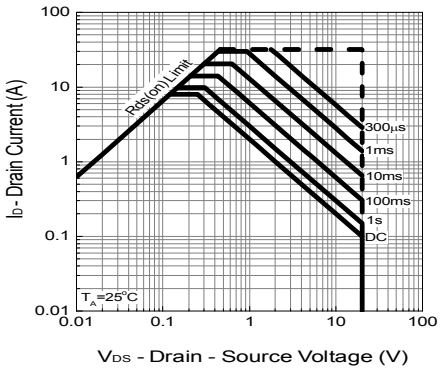
Power Dissipation



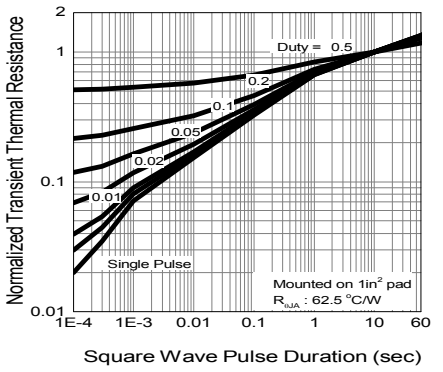
Drain Current



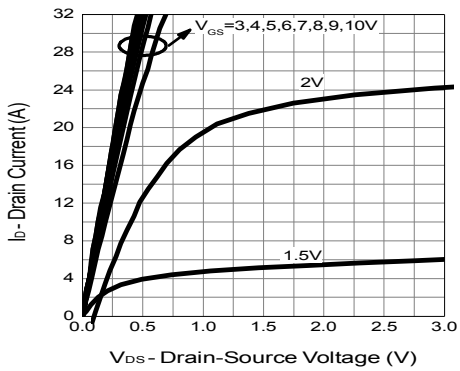
Safe Operation Area



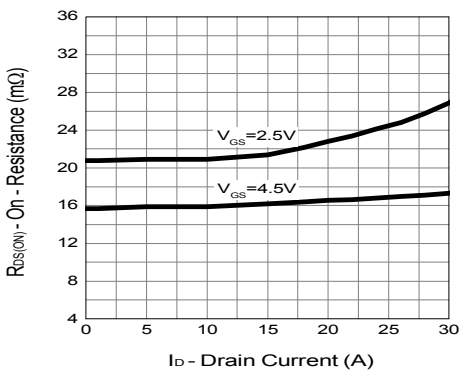
Thermal Transient Impedance



Output Characteristics

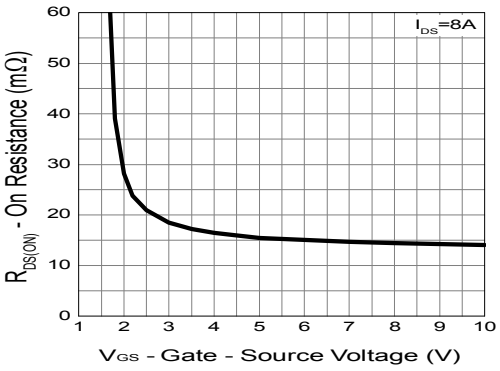


Drain-Source On Resistance

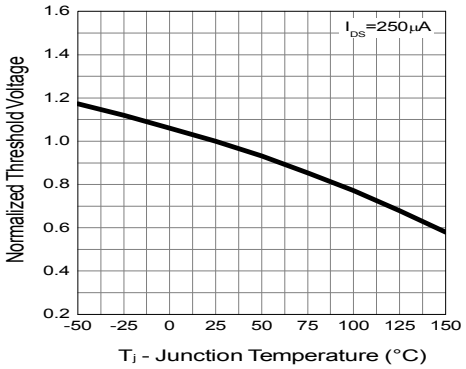


■ *TYPICAL CHARACTERISTICS (continuous)*

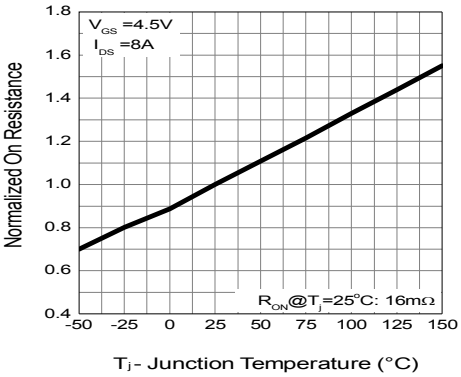
Transfer Characteristics



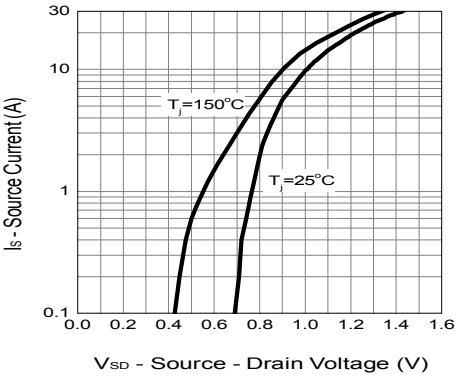
Gate Threshold Voltage



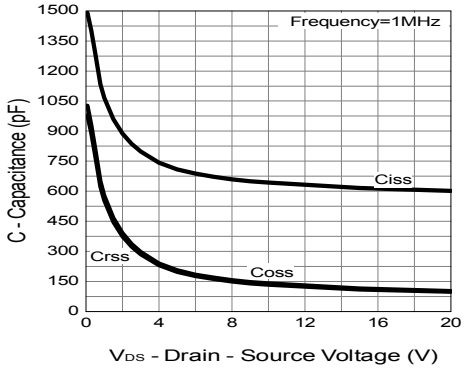
Drain-Source On Resistance



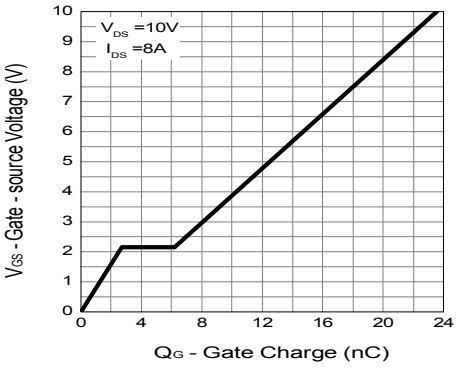
Source-Drain Diode Forward



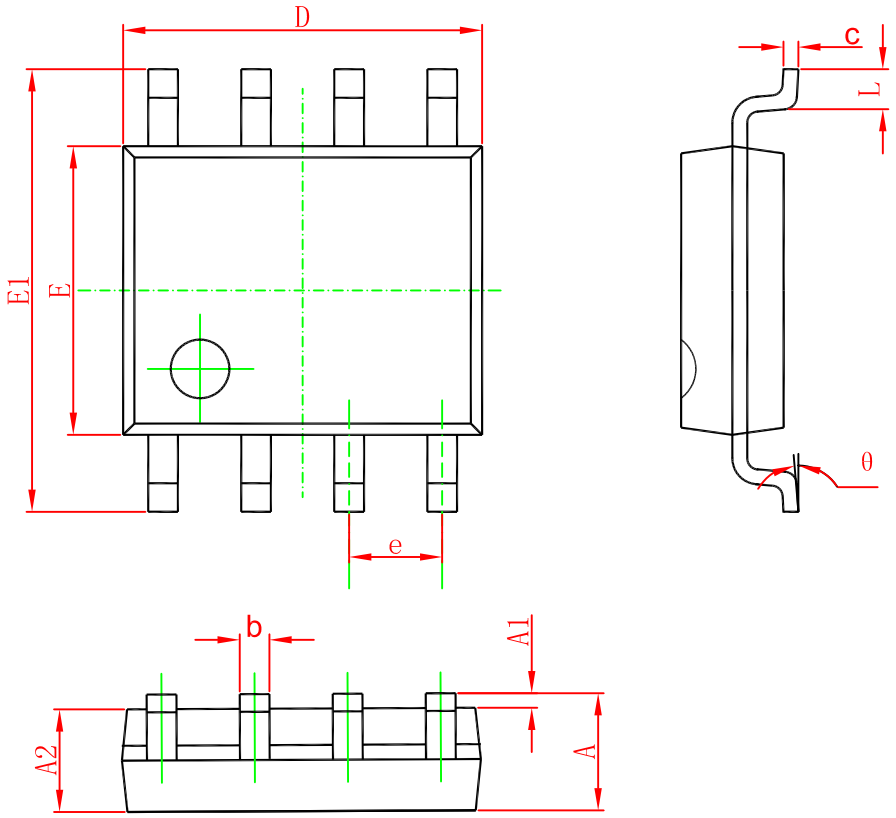
Capacitance



Gate Charge



■ *SOP8 PACKAGE OUTLINE DIMENSIONS*

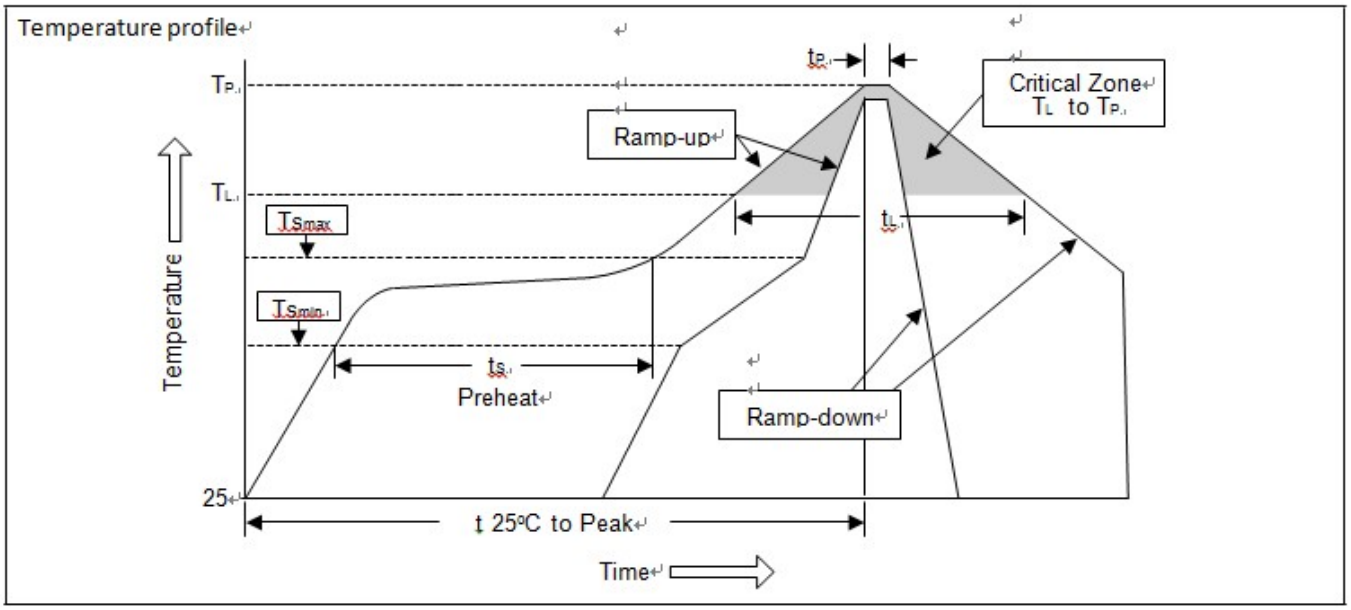


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.